



3. (20 points) Compute the following additions assuming the numbers are 2's complement numbers. Show the result, and indicate which, if any, cause overflow.

$$\begin{array}{r} \text{A) } 10111001 \\ + 11010110 \\ \hline \end{array}$$

$$\begin{array}{r} \text{B) } 01011101 \\ + 00100001 \\ \hline \end{array}$$

$$\begin{array}{r} \text{C) } 00100110 \\ + 01011110 \\ \hline \end{array}$$

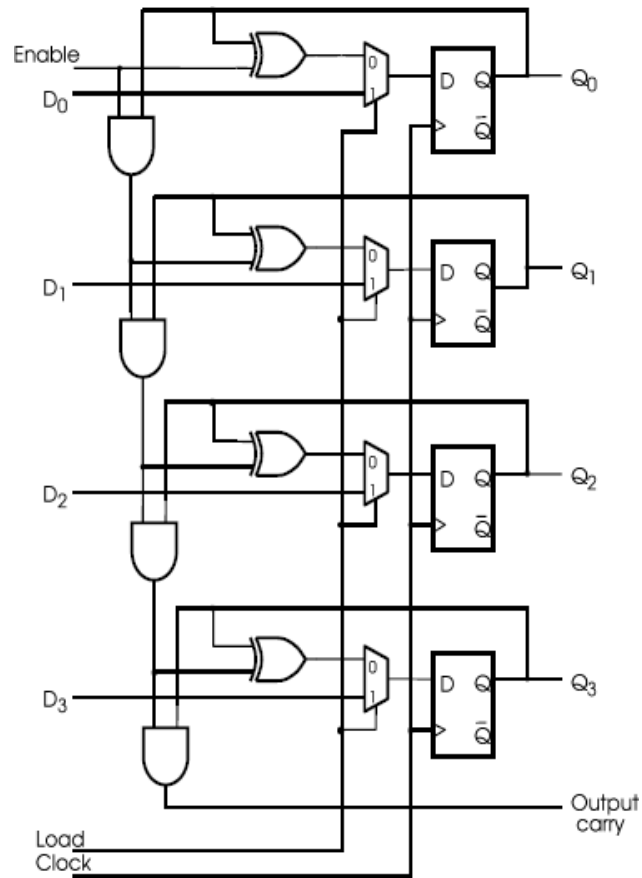
$$\begin{array}{r} \text{D) } 01001010 \\ + 11110110 \\ \hline \end{array}$$

$$\begin{array}{r} \text{E) } 10010110 \\ + 01001101 \\ \hline \end{array}$$

4. (20 points) Design a finite state machine with one input  $I$ , and two outputs  $Z$  and  $E$ . The machine should produce a  $Z$  output whenever it has seen a 110 pattern on the input stream, except that if it ever sees a 001 pattern on the input stream, it should assert the  $E$  output, and keep that  $E$  output asserted until the machine is reset. Note that  $Z$  should never be asserted again once  $E$  is asserted. Design a state machine to implement this function. Don't implement the circuit, just draw the state diagram for a Moore-style state machine (i.e. outputs are determined only by the current state).

5. (20 points) Consider the counter circuit in the following figure, which is a synchronous counter with parallel load. Assume that  $T_{SU}$  (setup time) is 3ns and  $T_H$  (hold time) is 1ns for the flip flops. Assume that  $T_{pd}$  (propagation delay) through each gate (AND, XOR, and MUX) is 1ns.

What is the maximum clock frequency for which the counter will operate correctly? Why?



6. (20 points) Convert the following circuit to an equivalent circuit that uses only NAND gates. Do NOT minimize or optimize the circuit, just change the gate types. Apply deMorgan's theorem  $\overline{A \wedge B} = \overline{A} \vee \overline{B}$ .

