

Domino Static Gates

Final Design Report

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Abstract

Static circuit gates are the standard circuit devices used to build the major parts of digital circuits. Dynamic gates, such as domino circuits, are only used in certain sections of the circuit where speed is critical. These gates achieve higher speed compared to static gates at the cost of reduced noise margins. We propose a novel gate structure that tries to improved noise margin when compared to dynamic domino gates with a standard keeper while retaining some advantage over static gates in terms of performance and switching energy. Here we make a comparison between static, dynamic domino, dynamic domino with noise tolerant precharge and our novel domino static gates in terms of noise, switching energy and transition delay.

Motivation

Dynamic domino gates are able to achieve lower delays and less switching energy when compared to static gates because of their ability to source substantially more output current for the same input load capacitance. This is because, by design, the less effective PMOS gates are not connected to the inputs that drive the output low and there is only a single PMOS transistor for driving the output high. This configuration achieves further power reductions due to the reduced contention between the pull-up and the pull-down sections of a domino gate, since the pull-up and pull-down sections of the gate are not switched on simultaneously. The

drawback of this design is that the output node is left floating for some time making it susceptible to noise and reduces the usability of the gate. Hence improving noise margins will allow domino gates to be more robust and increase their usable design space. Improving the noise margin will affect other important parameters like delay, power and size of the circuit. Understanding the tradeoff between performance, noise and energy is necessary to optimize the design of these gates given their particular circuit environment and demands. The a new gate topology tried in this project has characteristics of both static combinational gates and dynamic domino gates.

We do some characterization of input noise of the gate in terms our three critical parameters: performance, noise and energy. The results of our new circuit topology are compared against our benchmark of static gates, domino gates with NTP and domino gates.

Introduction

Static gates are those in which the output is always driven with a low impedance path to either power or ground. A combinational static gate is one in which the path is exclusively driven by input signals to the gate. In order to achieve this, the path to power is the dual or complement of the path to ground. Each input will therefore drive both PMOS and NMOS transistors. Since domino gates have independent paths to power and ground, most of the inputs do not drive both PMOS and NMOS transistors. In domino gates,

the path to power and ground only need to be asserted to flip the state of the output from high to low and vice versa. When the path to power or ground is not asserted, the output is floating. In these states the output is dependent on its previous state.

The floating output node of the dynamic domino gate makes it very vulnerable to noise and causes its noise margin to be heavily dependent on the threshold voltage whereas the noise margin of static gates is higher. Scaling results in reduced supply voltages and this increases the effect of noise as the ratio of noise to rail voltage increases. This is further compounded by the fact that threshold voltage has not scaled well and the resulting reduction in the difference between the threshold voltage and the rail voltage.

Some techniques used to increase the noise margin of domino gates while retaining some of their advantage of speed and lower switching energy compared to static gates have been illustrated in Figure 1 and discussed below.

1. *Keeper transistors:* This circuit structure is shown in Figure 1(a). This circuit is a simple feedback circuit consisting of two inverters to maintain the output at its previous state despite the noise and charge sharing in dynamic domino circuits. This feedback circuit does not leave the output node floating and provides a pull-up or pull-down path for the output at all times. This provides a path for the output node to recover from the effects of noise and thus increases the noise margin. This structure also results in contention between the pull-up structure of the dynamic gate and the pull-down structure of the feedback and vice versa causing an increase in switching energy and reduced speed. In some cases, the pull-down section of the feedback (shown within the box) is omitted as keeping the output low is not considered important.

2. *Noise Tolerant Precharge (NTP) circuit:* This circuit structure is shown in Figure

- 1(b). This circuit structure basically provides a weak pull-up structure along with the dynamic gate resulting in the implementation of $f(x) + \overline{pch}$ where $f(x)$ is the function implemented by the pull-down structure of the dynamic gate. This circuit does not have a feedback and does not need an additional pull-down structure. This structure essentially forms a static gate with an additional pull-up path \overline{pch} . Hence this circuit structure also suffers the same contention issues as in a static gate [1] [2].

3. *Domino Static Gate:* This is the novel circuit topology which is shown in Figure 1(c). This circuit structure aims at reducing the contention between the pull-up structure of the feedback and the pull-down structure of the dynamic gate and vice versa as seen in the gate structure using keeper transistors. This can help reduce the switching energy required and increase the speed of the gate. This gate structure can also be used to improve the noise margin and performance of the dynamic gate when used in the set/reset mode of operation and not just for clocked operation like the NTP topology discussed above. This structure will be discussed in more detail in the next section.

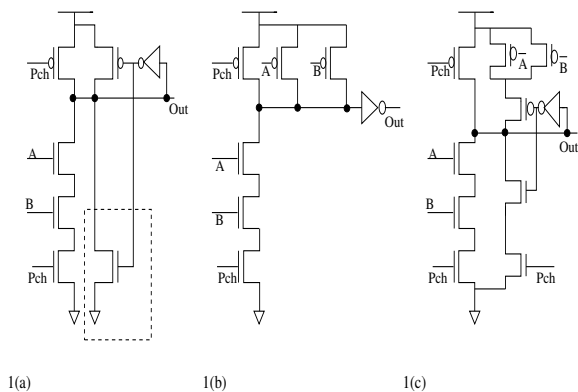


Figure 1: Different circuit topologies

Principle

The “static domino” circuits make a tradeoff in performance and noise by making the keeper statically controlled by the inputs.

Keeper Power and Performance Issues

A keeper circuit is used to keep the previous output asserted on the output node of a dynamic gate in the dynamic state. Unfortunately this circuit also creates contention between pull-up and pull-down structures in a domino gate when it switches. When the signal at the output is low, it is kept low in the dynamic state by the NMOS transistor of the feedback as shown in Figure 2(a). When the precharge signal goes low, the PMOS transistor pulls the output to a high. This pull-up action has to fight the pull-down by the NMOS transistor in the feedback in order to get the output node to a high. The pull-up and pull-down actions have been indicated in Figure 2(a). Similarly, when the signal at the output is high then it is kept high in the dynamic state by the PMOS transistor of the feedback as shown in Figure 2(b). When the precharge signal goes high, inputs of the NMOS transistors of the dynamic gate can try to pull the output node to a low as long as they result in a path to the ground. This pull-down structure of the dynamic gate has to overpower the pull-up of the PMOS transistor in the feedback to switch the output of the gate. The pull-up and pull-down actions in this case have been indicated in Figure 2(b). In both cases, the power consumption increases due to the formation of a direct path between the rails for brief periods of time and also slows down the gate. The proposed technique reduces this contention as shown in Figure 3(a) and 3(b).

The Figures 3(a) and 3(b) show how the circuit was expected to improve the pull-down and pull-up ability of the dynamic gate respectively by considerably reducing the period for which a

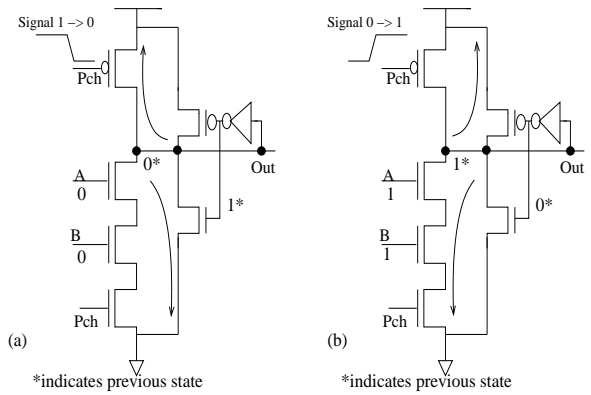


Figure 2: Issues with standard keeper shown with a 2 input NAND gate

direct connection between the rails exists. Figure 3(a) shows the case where the signal at the output is low and is being kept low in the dynamic state by the NMOS transistor of the feedback. When the precharge signal goes low, the PMOS transistor tries to pull the output node to a high. The contention between this pull-up structure and the pull-down structure of the feedback is greatly reduced unlike the keeper structure as the NMOS transistor with the precharge signal as input in the feedback section is turned off. Similarly, when the signal at the output is high then it is kept high in the dynamic state by the PMOS transistor of the feedback. As in Figure 3(b), when the precharge signal goes high, the inputs of the NMOS transistors of the dynamic gate can try to pull the output node to a low as long as they provide a path to the ground. Here again the contention between the pull-down structure of the dynamic gate and the pull-up structure of the feedback is greatly reduced as the pull-up structure of the feedback is switched off by the PMOS transistors having a complementary structure to that of the pull-down structure of the dynamic gate having the same inputs as the latter.

Noise and Performance Tradeoff

The noise margin of the gate will be determined by the amount of current that the keeper logic

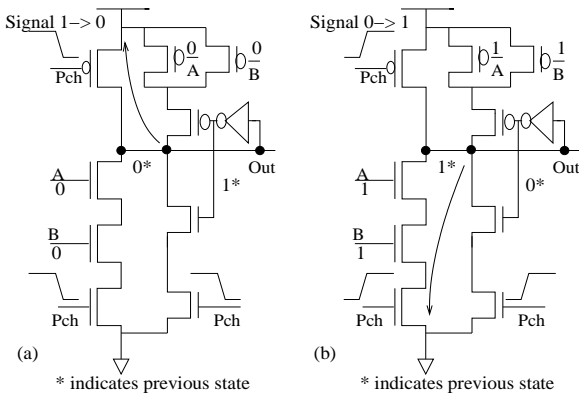


Figure 3: Expected behavior of proposed topology shown with a 2 input NAND gate

can source to overcome noise. Increasing the size of the keeper will increase the current and therefore, the margin of the gate. However, enlarging the keeper increases the switching energy and reduces the performance of the gate due to two factors:

1. reduced effective drive current of the pull-up or pull-down tree
2. increased load and gate parasitics increase the logical effort and decreases the gain of the gate

Experimental Setup

An example of the type of setup used to obtain the results for static gates, domino gates with standard keeper, domino static gates and domino gates with noise tolerant precharge is shown in Figure 4(a), 4(b), 4(c) and 4(d) respectively. In the circuits shown, the PMOS transistor of the dynamic gate has been sized to have a lower drive capability than the pull-down structure. This is usually the case when domino gates are used in the clocked environment. In the circuits shown in Figure 4, the ratio of NMOS to PMOS transistors has been set as $\frac{3}{2}$. The size of the feedback transistors is set using a parameter 's' and is usually set such that these feedback transistors are a fraction of the size of the transistors

in the dynamic gate. In addition to this, the size of transistors in the dynamic gate of 4(b) and 4(c) are modified such that the total input capacitance remains the same in all the circuits shown in Figure 4.

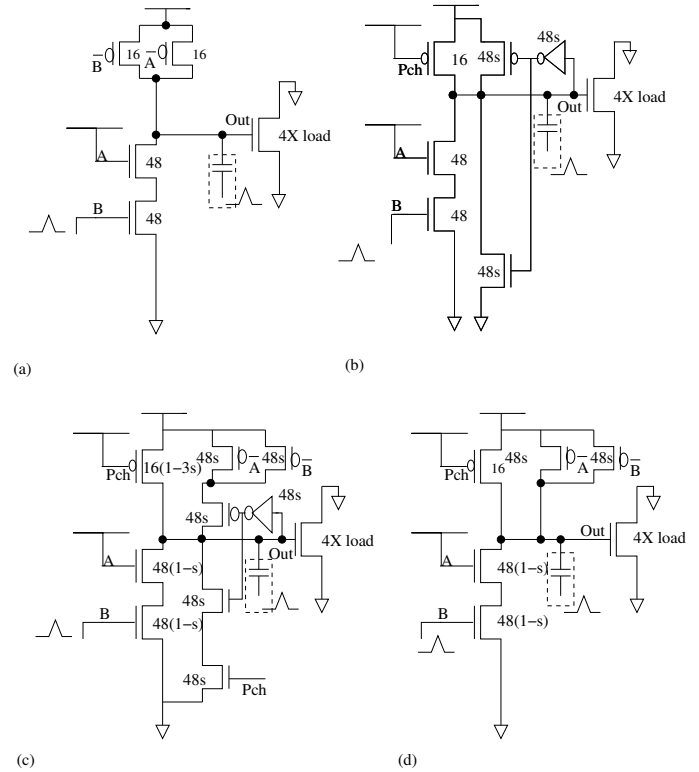


Figure 4: Experimental setup shown with 2 input NAND

Circuit Characterization Parameters

The parameters that I looked at look at are as follows:

1. **Performance** This parameter is determined in terms of the delay between 50% change in the input to a 50% change in the output. The increased performance of domino gates over static gates are the primary reason for their use. As we increase noise immunity of our domino gates, the performance degrades. Once performance

has degraded to the point that a domino gate is no longer faster than a static gate, it is no longer attractive. Therefore the rate of change in the performance and noise margin is very interesting.

2. **Switching Energy** This parameter is determined by measuring the energy consumed during the switching of the output from low to high and vice versa. This was done by measuring the RMS current during the switching period and multiplying this value with the supply voltage.
3. **Noise Margin:** This parameter determines the amount of variation in the input or output nodes that can be safely handled by the circuit without failing. A domino gate will fail if it flips state or produces non-monotonic output changes. For the purposes of this work, I adopted a more aggressive definition of failure under noise, which is a switch on the output voltage that reaches a voltage of V_{th} (or $V_{dd} - V_{th}$ for high signals). Such a noise definition is compatible with the static gates and domino with NTP structure against which I have compared the domino static structure. The noise signal that generates the changes in output voltages was specified in terms of amplitude and duration of the noise pulse that does not cause a change in the output greater than V_{th} .

Some results

The graphs plotted using the data obtained from the simulations are shown in Figures 5 - 46. The 180nm process technology was used for the simulations and the value of 's' was varied between 0.1 and 0.9. Furthermore, all inputs other than the one closest to the ground were given a high input. The input closest to ground was shaped like a square pulse with a rise and fall time of 5ps and was varied in amplitude from 0 to 1.8V in steps of 0.05V. At each level

of input, the duration of the pulse for which the circuit failed as per the criterion given in the previous section was noted. This was used to plot the graphs given as a separate tar file.

For the graphs in Figures 33 – 46 the same input was changed to a saturated ramp with a rise time of 90ps which is the rise time of the output of an inverter driving a FO4 inverter as a load. The measured delay and energy are plotted against the parameter 's' in these graphs (stored in delay and energy directories). For the energy figures the energy consumed over a period of 1ns has been plotted and so this includes the switching energy along with static dissipation.

Conclusion

The graphs showing the noise margin of the different gates in different configurations in the Figures 5 – 11 show that the domino static gates do have lower noise margin than the other 3 topologies for the same value of s. This is most probably because the the pull-up and pull-down stacks of the domino static gate topology is greater than the other ones and this reduces the current sourcing ability of the pull-down/pull-up structure. As seen in the Figures 12 – 32 the noise margin with respect to the input goes up with increase in the value of 's'. This increase is the greatest in the case of NTP and Domino static topologies with the increase being slightly greater in the case of domino static gates.

In the Figures 33- 39 the change in delay of the gate with change in the value of 's' can be seen. These values seem to be highly dependent on the function being computed and varies significantly depending on that. These graphs seem to indicate that different topologies might be suitable for different functions.

From the Figures 40 – 46 it is hard to conclude much about the energy consumption by the different topologies and a different setup might be needed to find out more on that front. The future work that would help characterize these gates better are study of the effect of noise on the out-

put node and a better method of arriving at energy consumption values.

References

- [1] H. Yamada, T. Hotta, T. Nishiyama, F. Murabayashi, T. Yamauchi, and H. Sawamoto, *A 13.3ns Double-precision Floating-point ALU and Multiplier*, in Proc. Intl. Conf. Computer Design, 1995, pp. 466-470.
- [2] F. Murabayashi, H. Yamada, T. Yamauchi, T. Ido, T. Nishiyama, K. Shimamura, S. Tanaka, T. Hotta, T. Shimizu, and H. Sawamoto, *2.5V Novel CMOS Circuit Techniques for a 150MHz Superscalar RISC Processor*, IEEE J. Solid-State Circuits, vol. 31, no. 7, pp. 972-980, Jul. 1996.
- [3] David Harris, Genevieve Breed, Matt Erler, David Diaz, *Comparison of Noise Tolerant Precharge to Conventional Feedback Keepers for Dynamic Logic*, Great Lakes Symposium on VLSI, 2003.

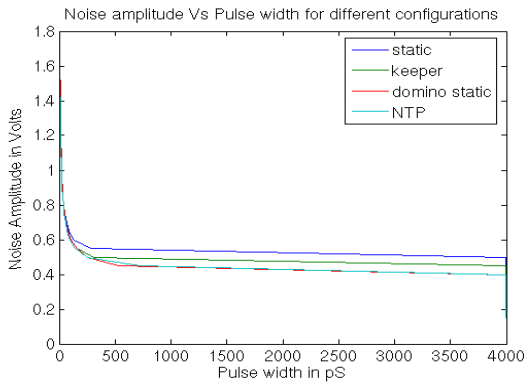


Figure 5: 2 input NAND with s=0.1

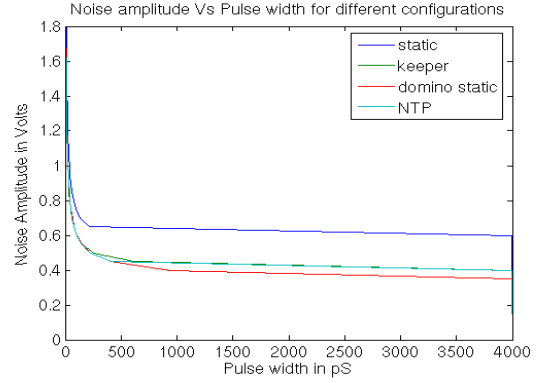


Figure 7: 2 input NOR with s=0.1

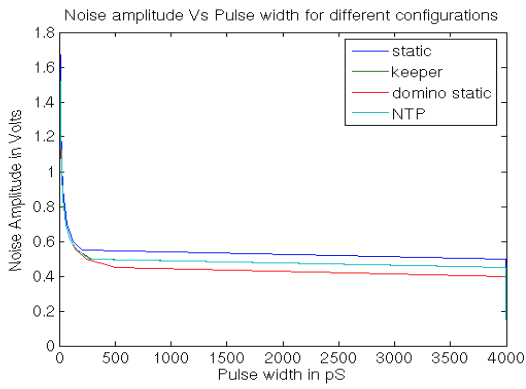


Figure 6: 3 input NAND with s=0.1

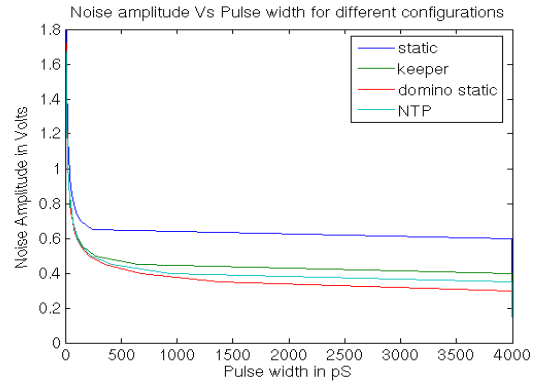


Figure 8: 3 input NOR with s=0.1

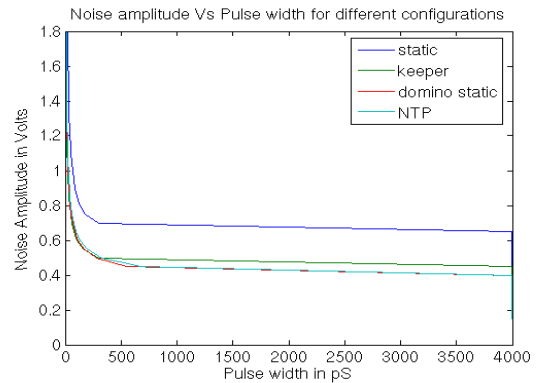


Figure 9: $F = a + bc$ with s=0.1

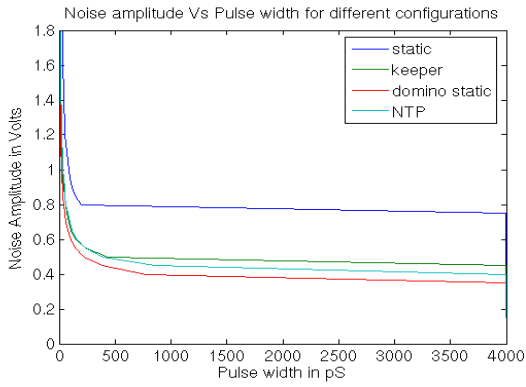


Figure 10: $F = \overline{a + bc + bd}$ input NAND with $s=0.1$

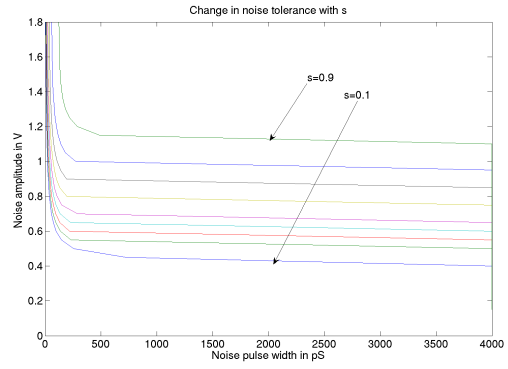


Figure 13: 2 input NAND with NTP and s varying from 0.1 to 0.9

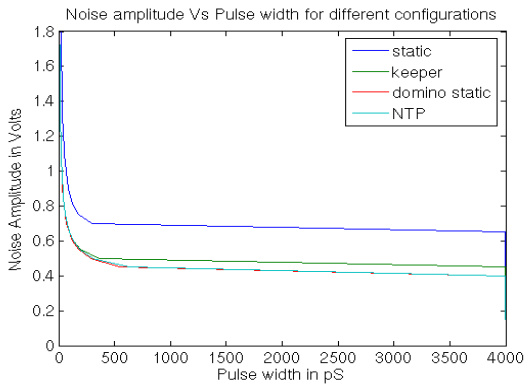


Figure 11: $F = \overline{ab + acd}$ input NAND with $s=0.1$

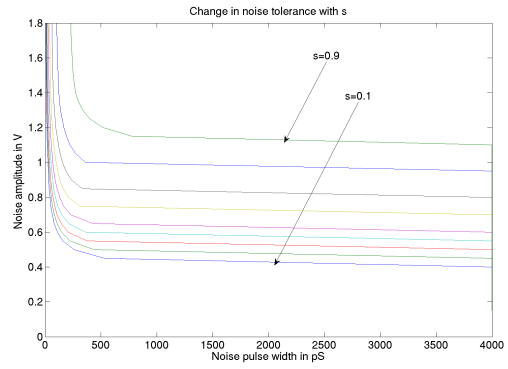


Figure 14: 2 input domino static NAND with s varying from 0.1 to 0.9

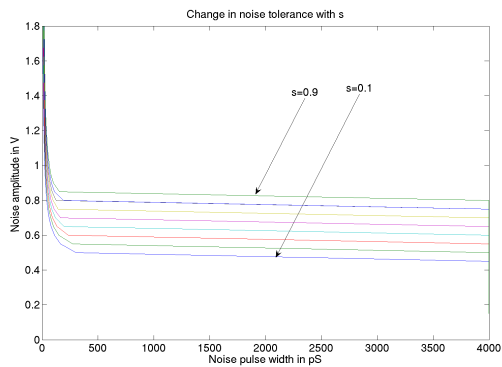


Figure 12: 2 input NAND with keeper and s varying from 0.1 to 0.9

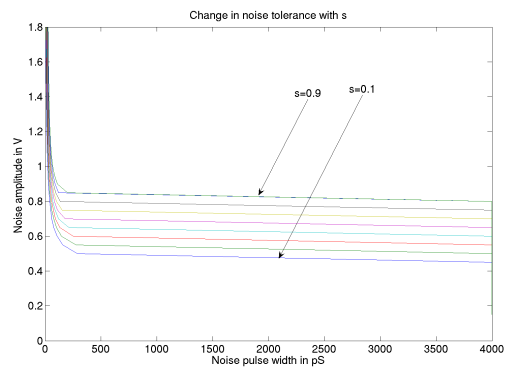


Figure 15: 3 input NAND with keeper and s varying from 0.1 to 0.9

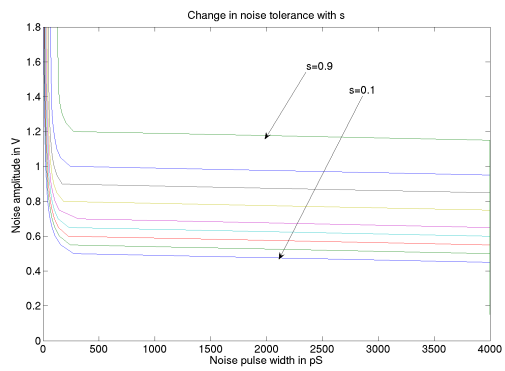


Figure 16: 3 input NAND with NTP and s varying from 0.1 to 0.9

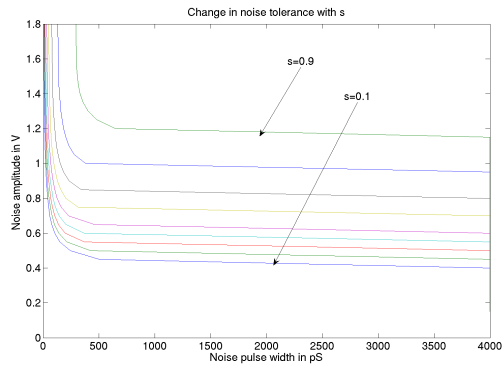


Figure 17: 3 input domino static NAND with s varying from 0.1 to 0.9

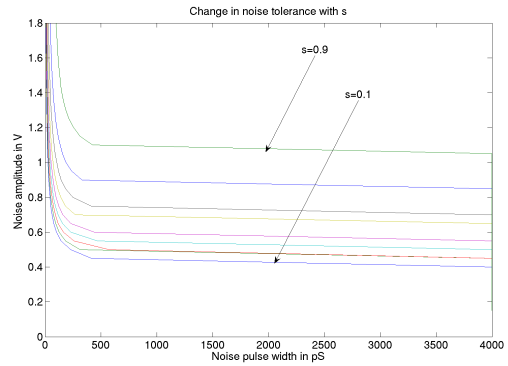


Figure 19: 3 input NOR with NTP and s varying from 0.1 to 0.9

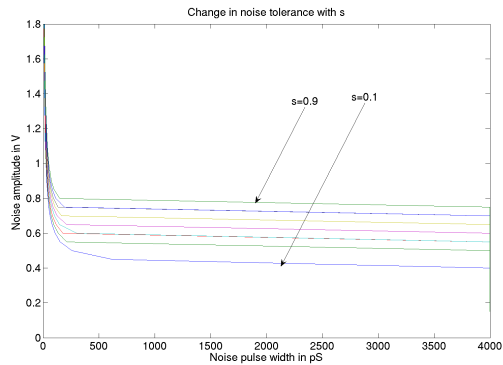


Figure 18: 2 input NOR with keeper and s varying from 0.1 to 0.9

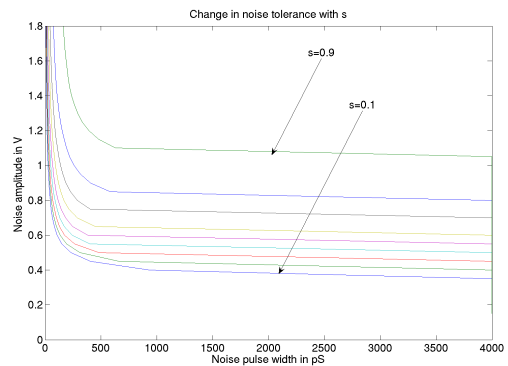


Figure 20: 2 input domino static NOR with s varying from 0.1 to 0.9

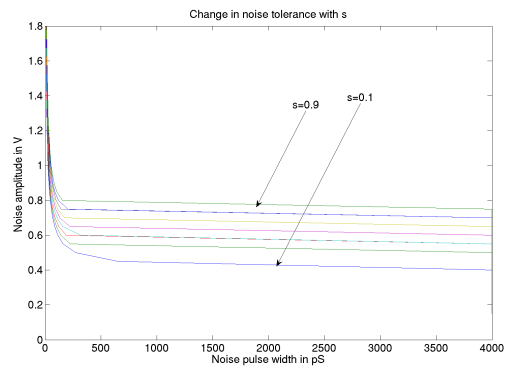


Figure 21: 3 input NOR with keeper and s varying from 0.1 to 0.9

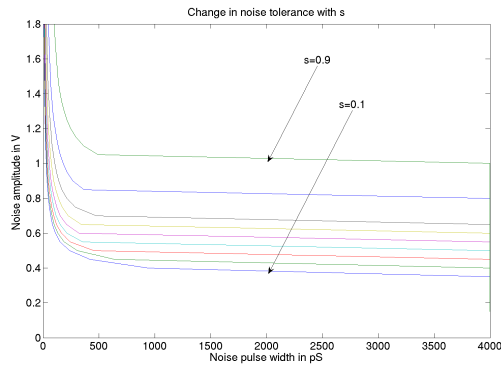


Figure 22: 3 input NOR with NTP and s varying from 0.1 to 0.9

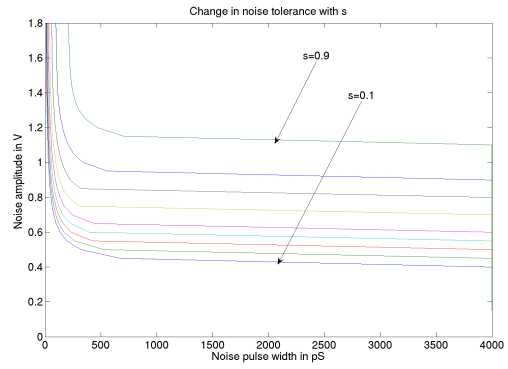


Figure 25: $F = \overline{a + bc}$ with NTP and s varying from 0.1 to 0.9

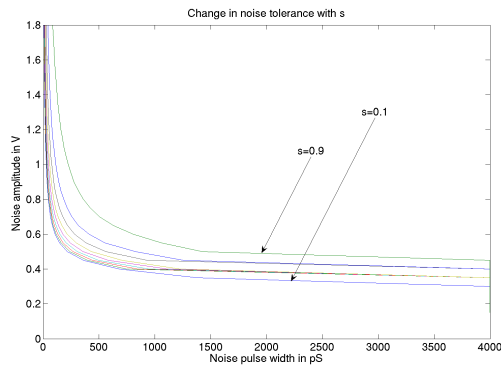


Figure 23: 3 input domino static NOR with s varying from 0.1 to 0.9

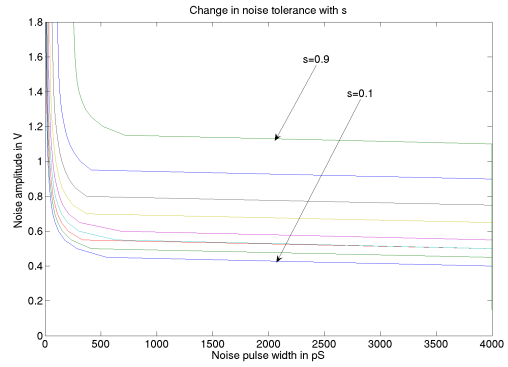


Figure 26: Domino static $F = \overline{a + bc}$ with s varying from 0.1 to 0.9

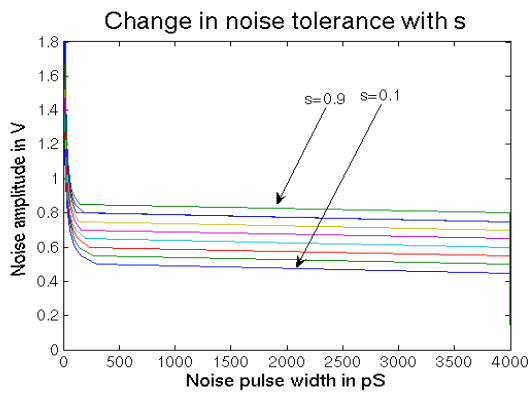


Figure 24: $F = \overline{a + bc}$ with keeper and s varying from 0.1 to 0.9

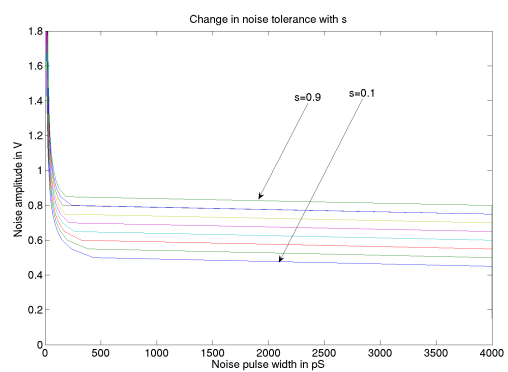


Figure 27: $F = \overline{a + bc + bd}$ with keeper and s varying from 0.1 to 0.9

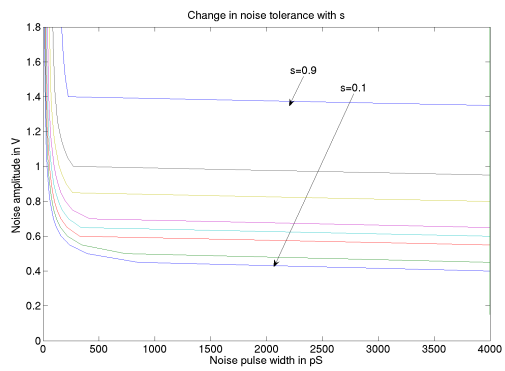


Figure 28: $F = \overline{a + bc + bd}$ with NTP and s varying from 0.1 to 0.9

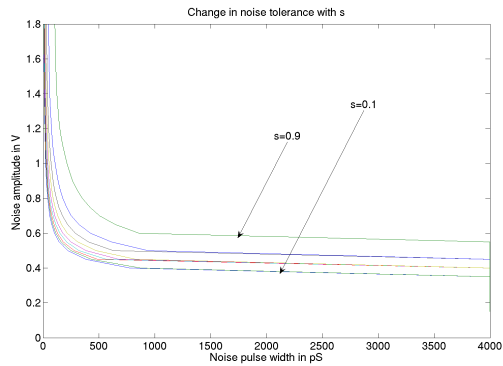


Figure 29: Domino static $F=\overline{a + bc + bd}$ with s varying from 0.1 to 0.9

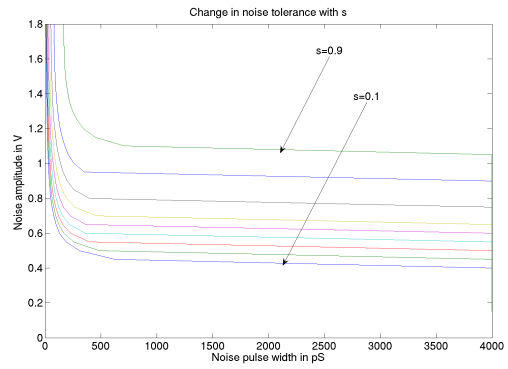


Figure 31: $F=\overline{ab + acd}$ with NTP and s varying from 0.1 to 0.9

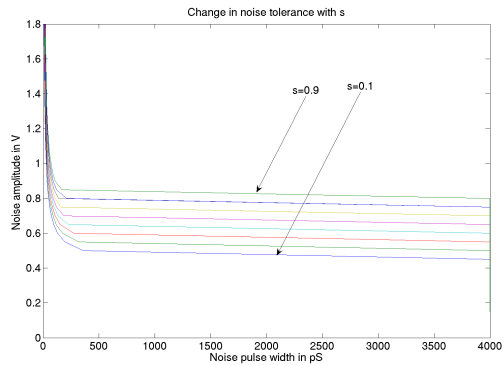


Figure 30: $F=\overline{ab + acd}$ with keeper and s varying from 0.1 to 0.9

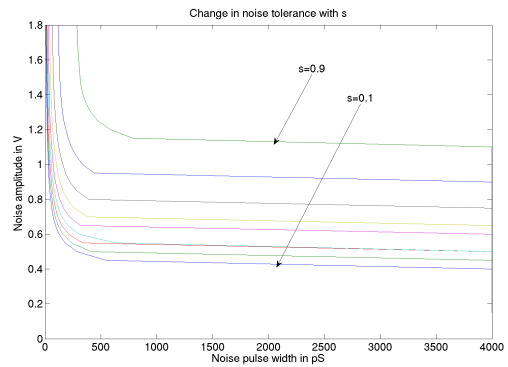


Figure 32: Domino static $F=\overline{ab + acd}$ with s varying from 0.1 to 0.9

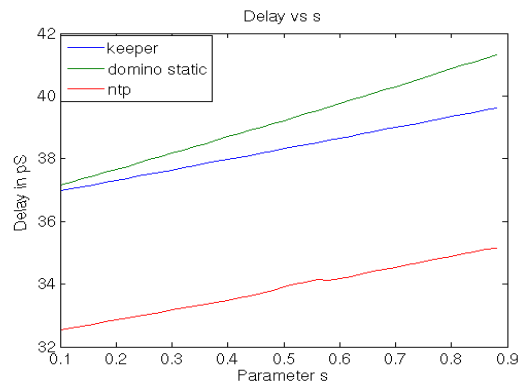


Figure 33: 2 input NAND with s varying from 0.1 to 0.9

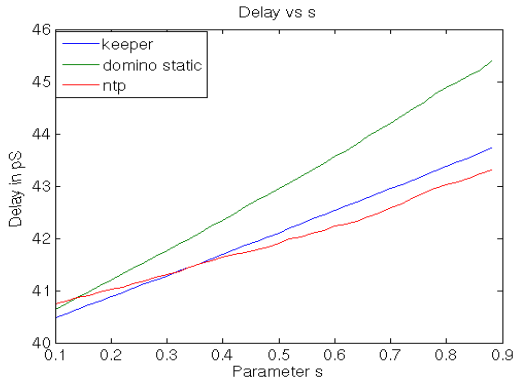


Figure 34: 3 input NAND with s varying from 0.1 to 0.9

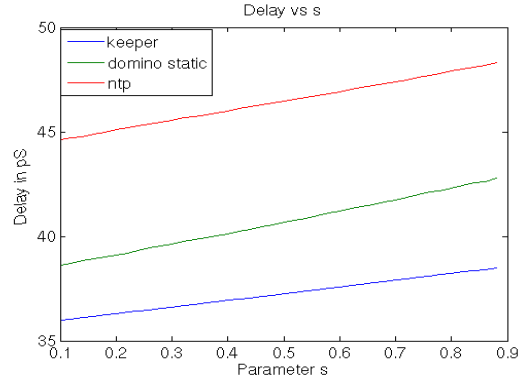


Figure 37: $F = \overline{a + bc}$ with s varying from 0.1 to 0.9

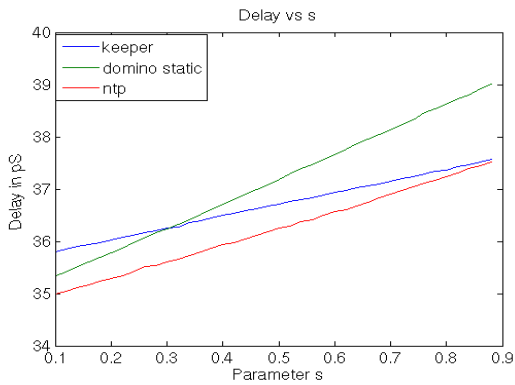


Figure 35: 2 input NOR with s varying from 0.1 to 0.9

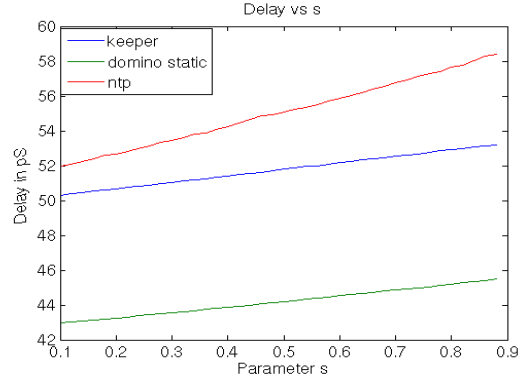


Figure 38: $F = \overline{a + bc + bd}$ input NAND with s varying from 0.1 to 0.9

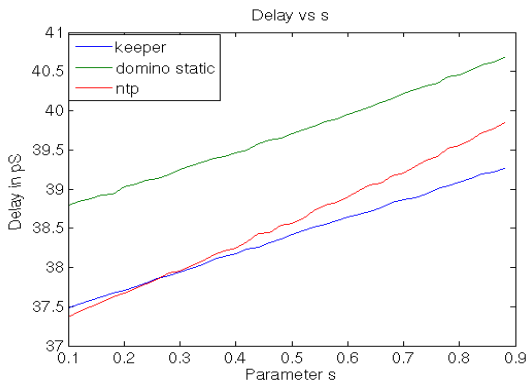


Figure 36: 3 input NOR with s varying from 0.1 to 0.9

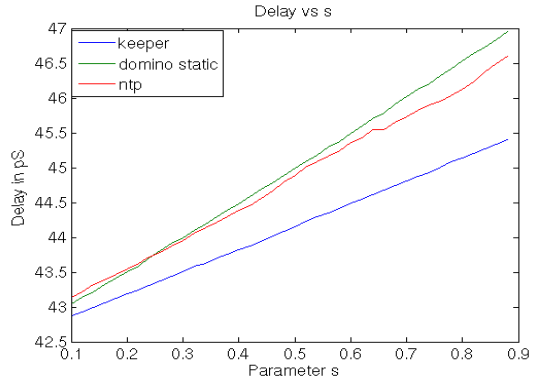


Figure 39: $F = \overline{ab + acd}$ input NAND with s varying from 0.1 to 0.9

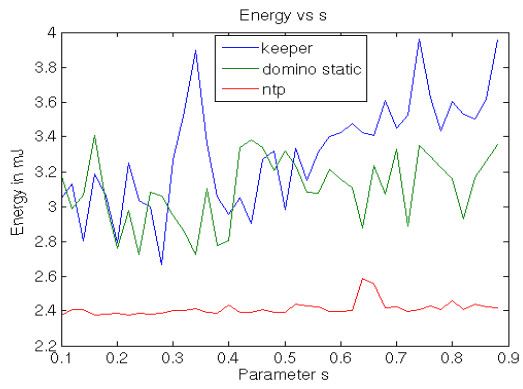


Figure 40: 2 input NAND with s varying from 0.1 to 0.9

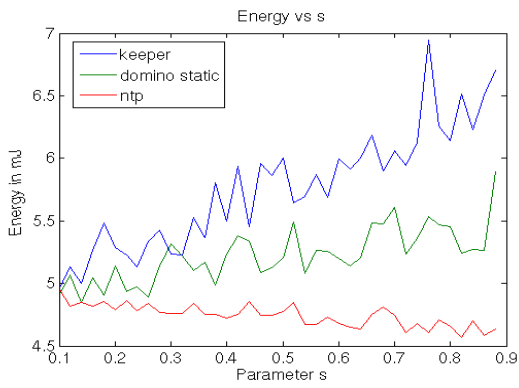


Figure 41: 3 input NAND with s varying from 0.1 to 0.9

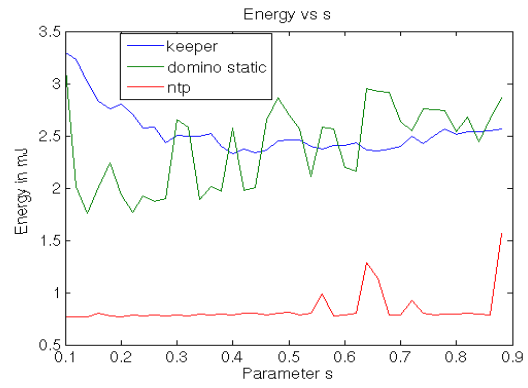


Figure 43: 3 input NOR with s varying from 0.1 to 0.9

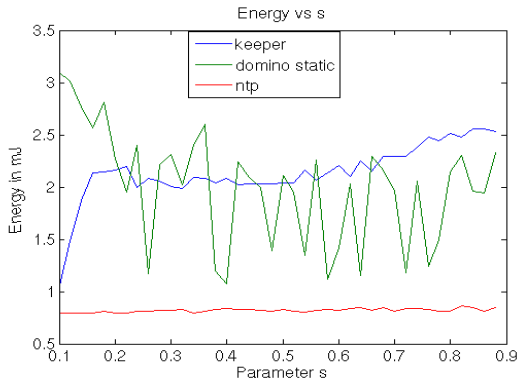


Figure 42: 2 input NOR with s varying from 0.1 to 0.9

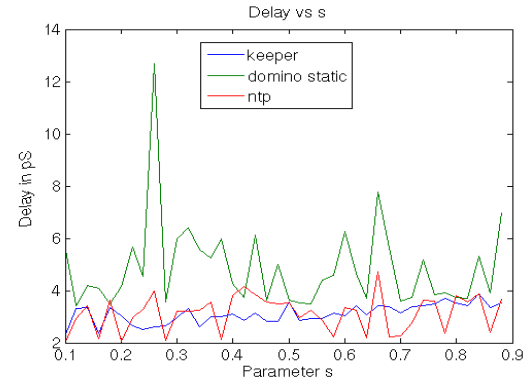


Figure 44: $F = a + bc$ with s varying from 0.1 to 0.9

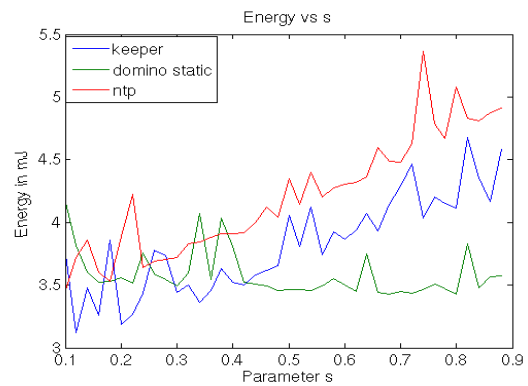


Figure 45: $F = a + bc + bd$ input NAND with s varying from 0.1 to 0.9

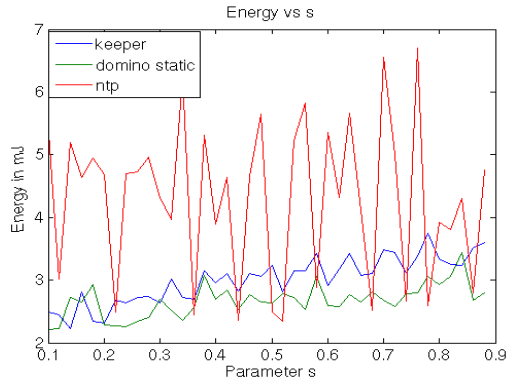


Figure 46: $F = \overline{ab + acd}$ input NAND with s varying from 0.1 to 0.9