

ECE 6770
Advanced Digital VLSI Design
Modifying P/N Ratios for Optimum Performance
Final Design Review
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Abstract: This project creates and characterizes gates with varying P/N ratios in the AMI 0.5 μm process. The ratios studied are 1, 1.5, 2, 2.5, and 3. Adders are constructed from the gates and characterized for speed and power. The adder's delay and power are used to determine the power-delay product, which was determined by this experiment to be the smallest for a P/N ratio of 2.

Introduction: In Digital VLSI Design class, the basic physics of CMOS logic cells are taught. When designing logic cells, the PMOS and NMOS transistors are designed to be equal in their drive strength, but this does not mean equal in transistor width. The reason for this is the PMOS transistor's charge carriers are different from the NMOS transistor's. NMOS transistors when turned on have an inverted channel filled with electrons, which are the majority carrier of this device in moving charge from source to drain. PMOS transistors have an inverted channel filled with holes, which have a lower mobility than electrons. The mobility of holes is one half to one third that of the mobility of electrons. To achieve the same drive strength, the digital logic cell designer must compensate for the lower mobility of holes by creating PMOS transistors with about twice the width of NMOS transistors. This term project studied the differences in switching speed and power with respect to P/N ratio.

The work: Three separate gates were tested for the different P/N ratios. These were Inverter, NAND, and XOR gates. The testing setups for the NAND and XOR gates are shown in Figure 1. A similar setup was done for the INV gate. The reason for the inverter on the input of each of the five gates is to cause the input slew to match the output slew of the gate.

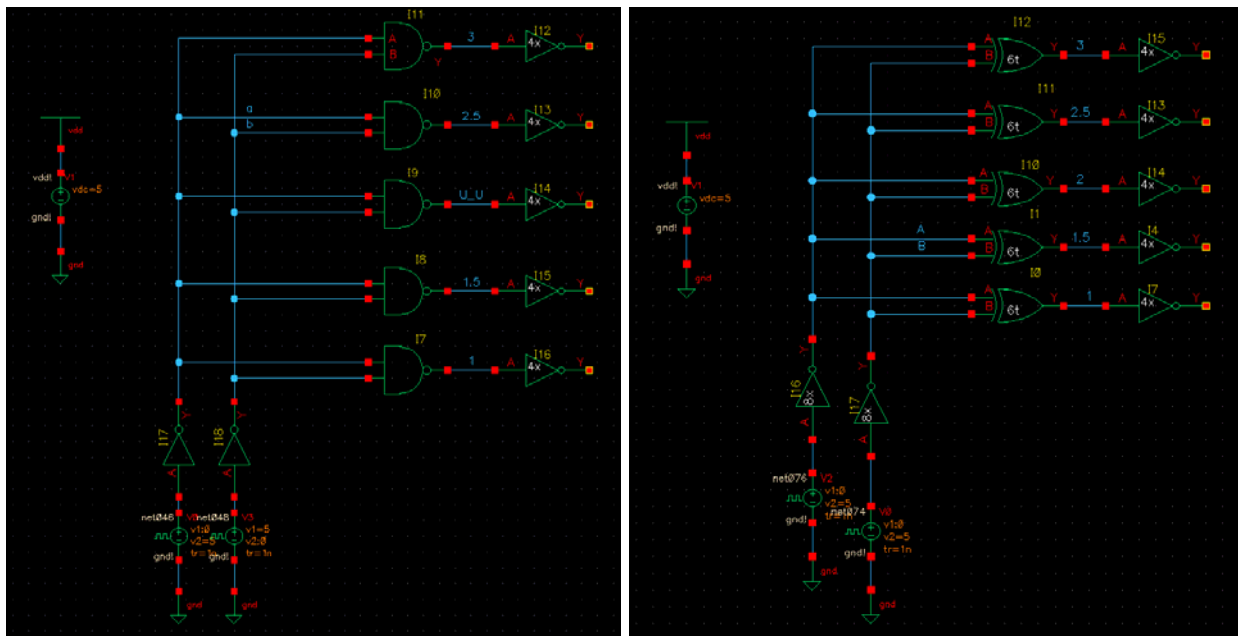


Figure 1: Test Setup for Testing Individual NAND and XOR Gates

The test results for the inverter, and NAND gates were collected separately for rise and fall times and delay times. Rise or fall time means 10% change to 90% change. Delay means 50% in to 50% out. Figure 2 and Figure 3 show the plots for the simulation of the inverter. Table 1 shows the results in tabular form, and Figure 4 shows the same results plotted against the P/N ratio.

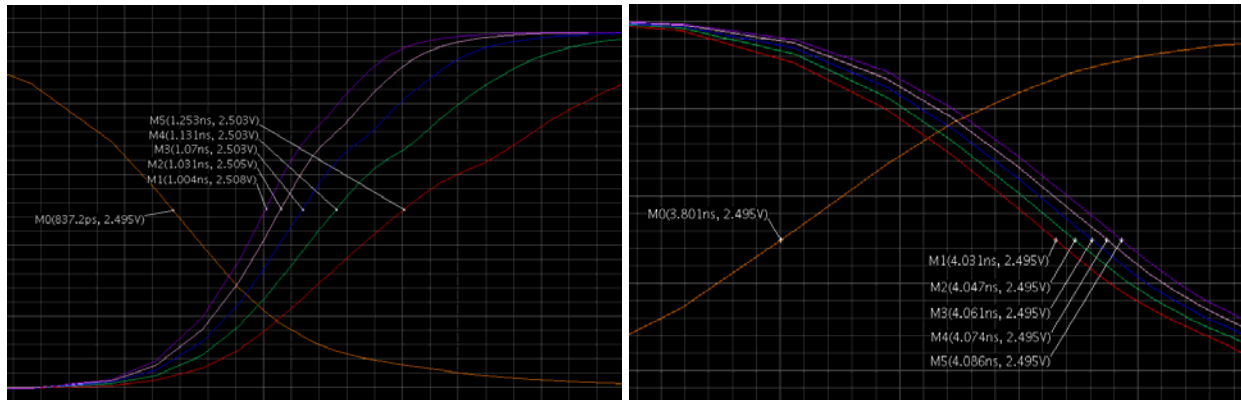


Figure 2: Inverter Rise and Fall Delay Simulations

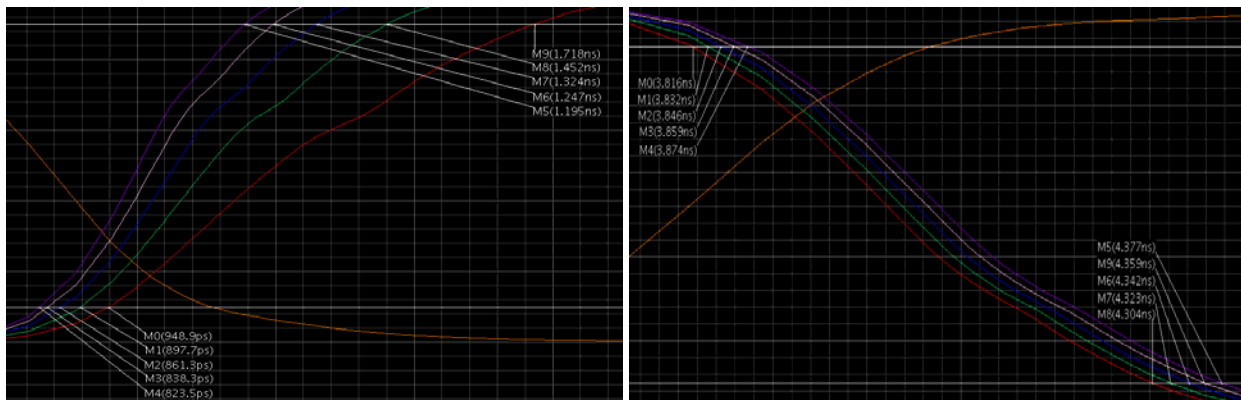


Figure 3: Inverter Rise and Fall Time Simulations

Inverter:

The fastest inverter gate appears from the average delay time to be the gate with aspect ratio of 3. This is not much of a surprise, since the NMOS transistor stays the same width, so the falling time stays somewhat constant. However, the rise time is drastically improved by widening the PMOS transistor.

Aspect Ratio	Rise Delay Time (ps)	Fall Delay Time (ps)	Rise time (ps)	Fall Time (ps)
1.0	416	230	769	488
1.5	294	246	554	491
2.0	233	260	493	496
2.5	194	273	409	500
3.0	167	285	372	503

Table 1: Inverter Rise and Fall Simulations

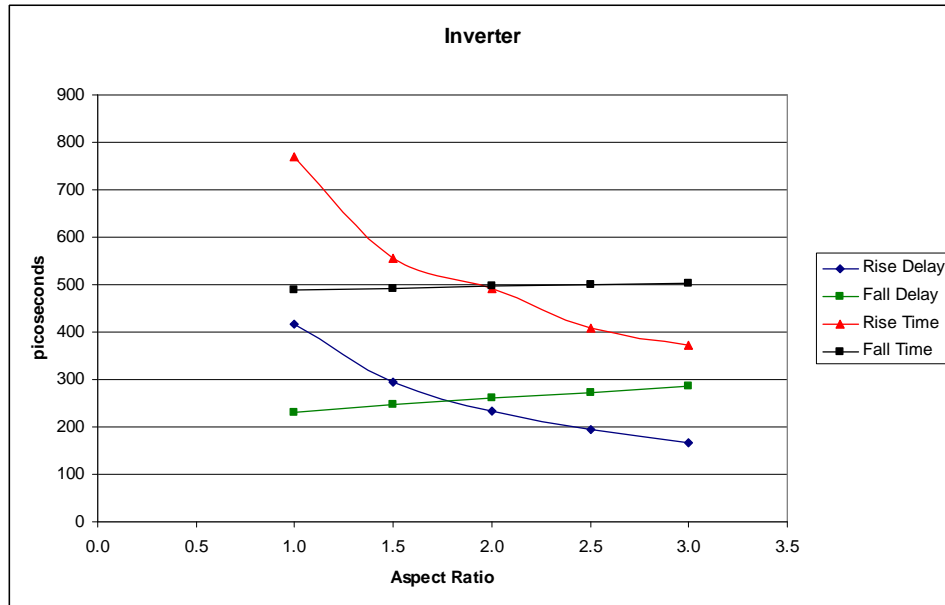


Figure 4: Inverter Simulation Results

NAND:

The NAND gate was tested in the same way as the inverter, although the single input switching and multiple input switching effects had to be taken into account. Multiple input switching occurs only 1 out of 4 times, so the single input switching is more important. The simulation results are shown in Table 2 and Table 3, and Figure 5 and Figure 6. Looking mainly at the single input switching table and plot, the fall delay remains more constant than the rising delay. Like the inverter, the average delay is least for the P/N ratio of 3.

Aspect Ratio	Rise Delay Time (ps)	Fall Delay Time (ps)	Rise time (ps)	Fall Time (ps)
1.0	347	263	561	588
1.5	246	300	479	572
2.0	182	328	436	570
2.5	139	353	405	573
3.0	107	375	387	571

Table 2: Multiple Input Switching NAND Gate

Aspect Ratio	Rise Delay Time (ps)	Fall Delay Time (ps)	Rise time (ps)	Fall Time (ps)
1.0	553	187	961	592
1.5	422	223	661	603
2.0	348	252	580	603
2.5	296	278	541	610
3.0	257	300	511	613

Table 3: Single Input Switching NAND Gate

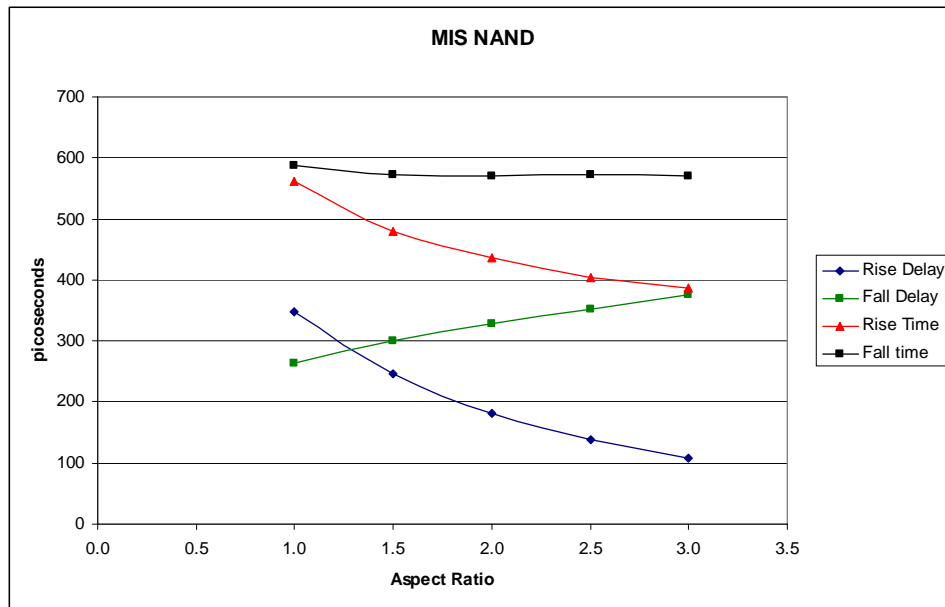


Figure 5: Multiple Input Switching NAND Results

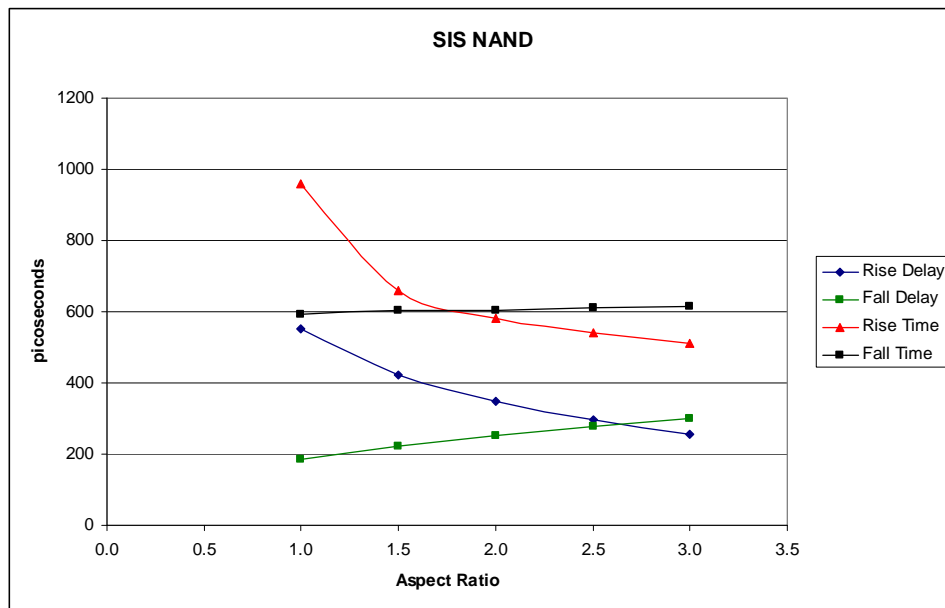


Figure 6: Single Input Switching NAND Results

XOR:

The XOR gate was tested in the same manner as the NAND and inverter gates, with the results plotted in Table 4 and Figure 7. Like the other two gates, the best XOR gate had ratio of 3.

Aspect Ratio	Average Rise Delay	Average Fall Delay	Max Rise Delay	Max Fall Delay
1.0	388	286	546	398
1.5	290	284	409	437
2.0	242	288	342	473
2.5	214	295	303	508
3.0	193	302	278	541

Table 4: XOR Rise and Fall Simulation Results

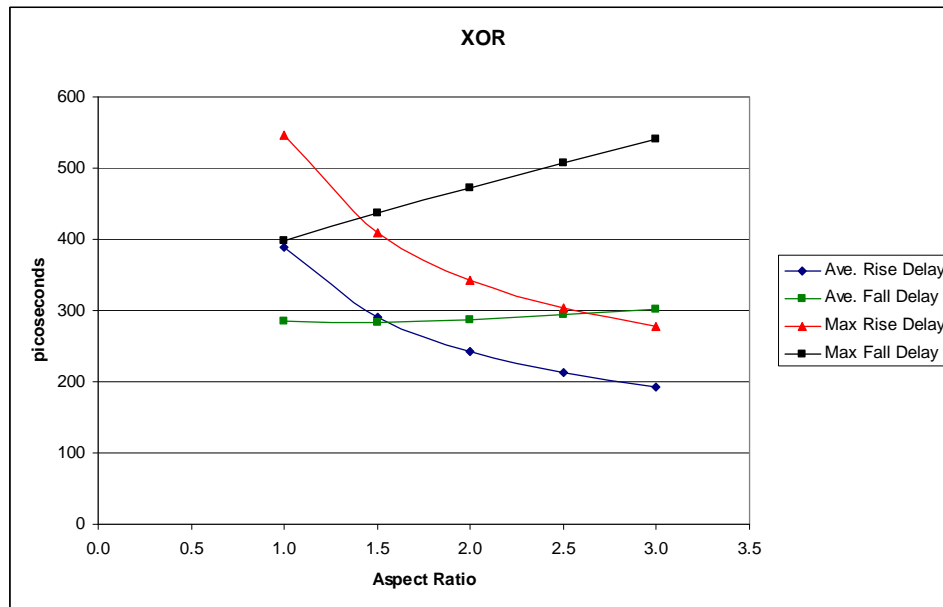


Figure 7: XOR Simulation Results

Adder:

The method to test the overall effects of modifying the P/N ratio was to create an adder. This was done with the schematic shown in Figure 8. However, the Cout line is created with three NAND gates instead of two AND gates and one OR gate. This can be done because of De Morgan's theorem, and will save some gate delays. When designing a fast adder, achieving minimum gate delays is important. Although for the testing purposes of this project the De Morgan's theorem wasn't necessary, it was useful in avoiding the creation of four copies of the OR gate.

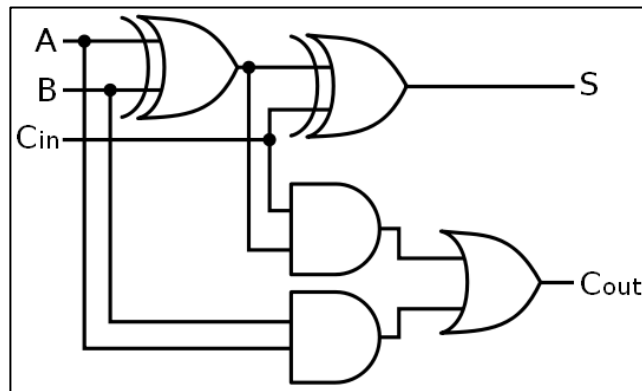


Figure 8: Full Adder Schematic

The adder was created five times using the different P/N ratioed gates, and replaced in the testing schematic shown in Figure 9. The full adder circuit was tested differently from the individual gates. The full adder's speed was tested only by delay time, and this was done for 20% in to 80% out of the gate. During the course of the project, this method was discovered as a more reliable method of testing for delay. Also, each possibility of switching from one input to another was tested, with a total of seven unique inputs producing a change in output. The switching delays are given in Table 5. The fastest adder, meaning the adder with the smallest maximum delay, is the adder with P/N ratio of 3. However, the adder with P/N ratio of 2.5 comes very close.

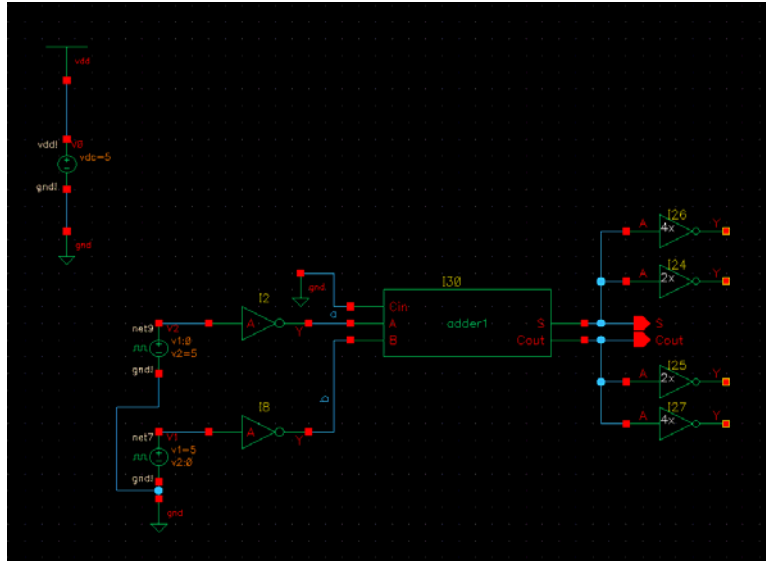


Figure 9: Full Adder Test Schematic

P/N Ratio	Delay1	Delay2	Delay3 (Cout,S)		Delay4	Delay5	Delay6 (Cout,S)		Delay7 (Cout,S)		Min Delay	Max Delay	Average Delay
1	0.96	2.63	1.24	1.01	0.645	2.32	1.28	1.11	0.74	2.59	0.645	2.63	1.61
1.5	0.98	1.97	0.92	1.11	0.655	1.78	0.92	1.2	0.78	1.97	0.655	1.97	1.38
2	0.97	1.77	0.7	1.16	0.64	1.6	0.72	1.26	0.76	1.76	0.64	1.77	1.31
2.5	0.97	1.68	0.7	1.22	0.65	1.51	0.72	1.34	0.76	1.67	0.65	1.68	1.29
3	0.99	1.67	0.67	1.32	0.69	1.5	0.68	1.43	0.78	1.66	0.67	1.67	1.32
Switching:	01-00	00-10	10-11		11-00	00-01	01-11		11-10		Delays in nanoseconds, 20% in to 80% out		

Table 5: Adder Switching Delays

In addition to delay testing, power testing was performed. Power was computed by switching the adders through a sequence of different inputs over a long period of time, and finding the average current flowing from the power supply. This is multiplied by the supply voltage to give a power reading. Because each adder was simulated with the same sequence for the same period of time, these power computations represent a fair comparison between adder circuits. Although not meant to be exact or even approximate real power readings (results will surely vary depending upon input sequence and clock speed), they provide an accurate comparison between the five circuits because each performs exactly the same function using a different amount of energy. The power is shown in Table 6, and plotted along with the delay in Figure 10.

P/N Ratio	Power (mW)	Power-Delay (pW-s)	Quiescent Power (μ W)
1	3.70	5.96	0.52
1.5	3.38	4.66	0.52
2	3.31	4.33	0.53
2.5	3.46	4.47	0.53
3	3.64	4.81	0.54

Table 6: Adder Power

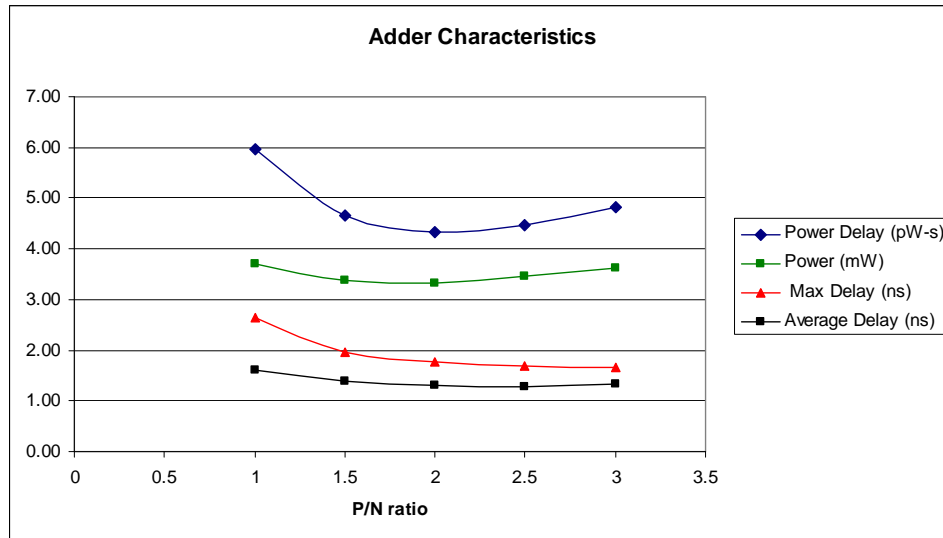


Figure 10: Adder Delay and Power Characteristics

Conclusion: The most important result of this project is the power-delay computation. This is given in Table 6, and plotted in Figure 10. A circuit's speed can be improved by increasing the width of the transistors, but this costs area and power. Sometimes, power and area are of no concern, but this is generally not the case. In a given technology, the optimum power-delay product is usually sought by designers to reduce power and delay.

As can be seen in Figure 10, reducing the size of the PMOS transistors will result in a large delay. Increasing the size of the PMOS transistors reduces the delay, but costs more power and area. Because simulating all gates in a cell library was not possible or within the scope of this project, the gates characterized here, and the adder circuit simulated makes a representation for the entire cell library. This project finds the optimum P/N ratio to be 2.0, based upon the power-delay product. This result is only valid for the AMI 0.5 μm process. The optimum ratio may change for other processes for which there are various differences in parasitic capacitance, charge carrier mobility, and threshold voltage.